WHAT IS CLAIMED IS:

1. A method for activating a plurality of rows of a memory device, the method comprising:

activating a predefined number of the rows in response to a single externally applied refresh command, wherein the predefined number is at least two of the plurality of rows.

2. The method of claim 1, wherein the predefined number is less than all of the plurality of rows.

3. The method of claim 1, wherein the externally applied refresh command is an auto-refresh command.

4. The method of claim 1, wherein the externally applied refresh command is an auto-refresh command issued by a memory controller.

5. The method of claim 1, wherein activating the predefined number of the rows comprises sequentially activating the predefined number of the rows.

6. The method of claim 1, wherein activating the predefined number of the rows is done without an oscillator internal to the memory.

7. The method of claim 1, wherein the externally applied refresh command is an auto-refresh command and wherein the predefined number is between two and four.

8. A method for activating rows of memory cells in a memory device comprising N rows of memory cells, the method comprising:

issuing auto-refresh commands at a first frequency; and

in response to the auto-refresh commands, activating rows of the memory at a second frequency greater than the first frequency.

9. The method of claim 8, wherein the first frequency is determined by the time needed to refresh a number of the rows at the second frequency.

10. The method of claim 8, wherein the auto-refresh commands are issued by a memory controller.

11. The method of claim 8, further comprising issuing a self-refresh command to place the memory device in a self-refresh mode.

12. The method of claim 8, further comprising, in response to each auto refresh command, activating a predetermined number of rows of memory, the predetermined number being greater than two.

13. A method of activating rows of memory to be refreshed, comprising:

initiating a first row activation of a first row in a memory array;

in response to the row activation signal, invoking a first timing circuit to issue a first refresh_end signal signaling an end of the first row activation after a period of time;

in response to the refresh_end signal, invoking a second timing circuit to issue a refresh signal; and

initiating a second row activation of a second row in the memory array in response to refresh signal.

14. The method of claim 13, further comprising disabling the second timer after the refresh signal is issued.

15. The method of claim 13, further comprising disabling the second timer during self-refresh of the rows of memory.

16. The method of claim 13, further comprising in response to the second row activation signal, invoking the first timing circuit to issue second refresh_end signal signaling an end of the second row activation after the period of time.

17. A refresh timing circuit for a memory device, comprising:

a first timer configured to issue a Refresh_End signal a period of time, t1, after receiving each row activate signal from a control circuit; and

a second timer configured to receive the Refresh_End signals from the first timer and issue a refresh signal a period of time, t2, after receiving each Refresh_End signal, wherein the refresh signal causes the control circuit to issue at least a second row activate signal.

18. The circuit of claim 17, wherein the first row activate signal is received by the first timer in response to an externally applied auto-refresh command being received.

19. The circuit of claim 17, wherein the device is a memory array.

20. The circuit of claim 17, wherein the second timing circuit comprises a latch configured to output the refresh signal when the latch is set and a feedback line on which the refresh signal is propagated back to the latch to reset the latch and prevent a subsequent Refresh_End signal from causing issuance of a subsequent refresh signal.

21. A on-chip circuit for refreshing a memory device, comprising:

a control circuit comprising:

a command line for receiving externally initiated refresh commands; and

a row activate output line for issuing row activate signals, wherein the control circuit is configured to issue a first row activate signal in response to receiving an externally initiated refresh command on the command line;

a first timer coupled to the control circuit and configured to receive each of the row activate commands from the control circuit and issue Refresh_End signals a period of time, t1, after receiving each row activate signal; and

a second timer coupled to the control circuit and the first timer and configured to receive the Refresh_End signals from the first timer and issue a refresh signal a period of time, t2, after receiving each Refresh_End signal, wherein the refresh signal causes the control circuit to issue at least a second row activate signal.

22. The circuit of claim 21, wherein the command line is an auto-refresh command line.

23. The circuit of claim 21, wherein the second timer is configured to issue a disabling signal to disable the second timer.

24. The circuit of claim 23, wherein the disabling signal is the refresh signal.

25. An apparatus for activating rows of memory in a memory device, comprising:

a controller configured to issue auto-refresh commands;

a control circuit configured to issue at least sequential row activate signals to activate the rows of memory in the memory device; wherein a first row activate signal is issued in response to receiving a first auto-refresh command;

a first timer configured to receive each of the row activate signals from the control circuit and issue Refresh_End signals a period of time, t1, after receiving each row activate signal; and

a second timer configured to receive the Refresh_End signals from the first timer and issue a refresh signal a period of time, t2, after receiving each Refresh_End signal, wherein the refresh signal causes the control circuit to issue at least a second row activate signal to the first timer.

26. The apparatus of claim 25, wherein the control circuit, the first timer and the second timer are disposed on the memory device.

27. The apparatus of claim 25, further comprising a disabling circuit configured to disable the second timer while the memory device is in self-refresh mode.